



Low-Voltage, CMOS Analog Multiplexers/Switches

General Description

The MAX4581/MAX4582/MAX4583 are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4581), two 4-channel multiplexers (MAX4582), and three single-pole/double-throw (SPDT) switches (MAX4583).

These CMOS devices can operate continuously with $\pm 2\text{V}$ to $\pm 6\text{V}$ dual power supplies or a $+2\text{V}$ to $+12\text{V}$ single supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at $+25^\circ\text{C}$ or 5nA at $+85^\circ\text{C}$.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single $+5\text{V}$ or dual $\pm 5\text{V}$ supplies.

Applications

Battery-Operated Equipment
Audio and Video Signal Routing
Low-Voltage Data-Acquisition Systems
Communications Circuits
Automotive

Features

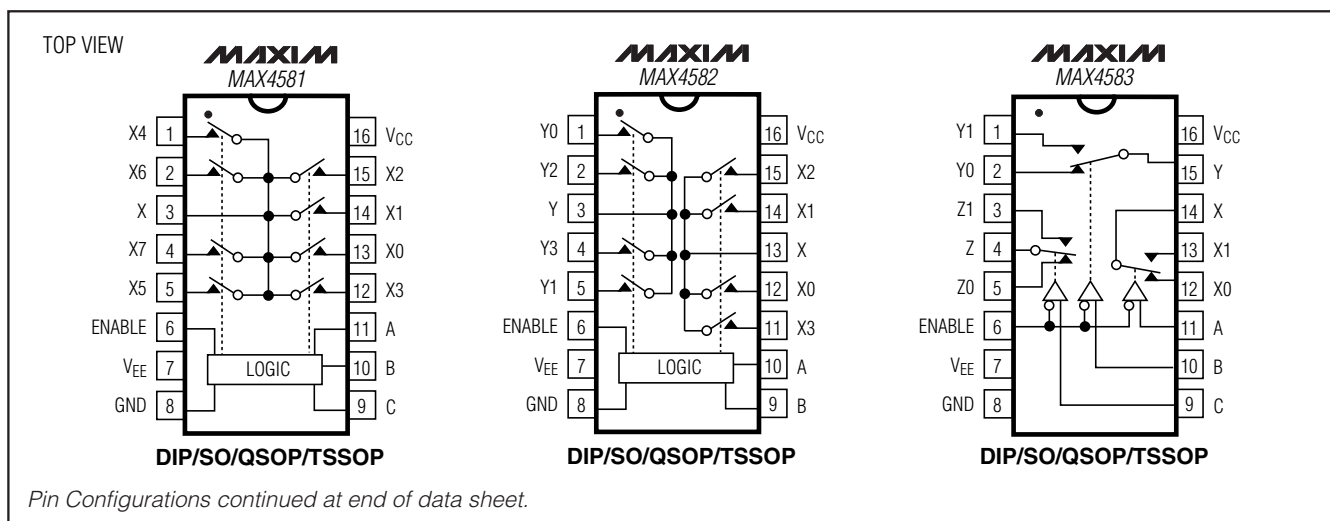
- ◆ Offered in Automotive Temperature Range (-40°C to $+125^\circ\text{C}$)
- ◆ Guaranteed On-Resistance
 80Ω with $\pm 5\text{V}$ Supplies
 150Ω with Single $+5\text{V}$ Supply
- ◆ Guaranteed On-Resistance Match Between Channels
- ◆ Guaranteed Low Off-Leakage Current
 1nA at $+25^\circ\text{C}$
- ◆ Guaranteed Low On-Leakage Current
 1nA at $+25^\circ\text{C}$
- ◆ $+2\text{V}$ to $+12\text{V}$ Single-Supply Operation
 $\pm 2\text{V}$ to $\pm 6\text{V}$ Dual-Supply Operation
- ◆ TTL/CMOS-Logic Compatible
- ◆ Low Distortion: $< 0.02\%$ (600Ω)
- ◆ Low Crosstalk: $< -96\text{dB}$ (50Ω , MAX4582)
- ◆ High Off-Isolation: $< -74\text{dB}$ (50Ω)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4581CPE	0°C to $+70^\circ\text{C}$	16 Plastic DIP	P16-1
MAX4581CSE	0°C to $+70^\circ\text{C}$	16 Narrow SO	S16-2
MAX4581CUE	0°C to $+70^\circ\text{C}$	16 TSSOP	U16-2

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams



Maxim Integrated Products 1

For pricing delivery, and ordering information please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX4581/MAX4582/MAX4583

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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V_{EE}

V_{CC} -0.3V to 13V

Voltage into Any Terminal (Note 1) ... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)

Continuous Current into Any Terminal ±20mA

Peak Current, X₋, Y₋, Z₋

(pulsed at 1ms, 10% duty cycle) ±40mA

ESD per Method 3015.7 >2000V

Continuous Power Dissipation (T_A = +70°C)

16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW

16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW

16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW

16-Pin TSSOP (derate 6.7mW/°C above +70°C) 457mW

16-Pin QFN (derate 18.5mW/°C above +70°C) 1481mW

Operating Temperature Ranges

MAX458_C_ 0°C to +70°C

MAX458_E_ -40°C to +85°C

MAX458_A_ -40°C to +125°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note 1: Voltages exceeding V_{CC} or V_{EE} on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V_{CC} = 4.5V to 5.5V, V_{EE} = -4.5V to -5.5V, V_H = 2.4V, V_L = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog-Signal Range	V _X , V _Y , V _Z			C, E, A	V _{EE}		V _{CC}	V
Switch On-Resistance	R _{ON}	V _{CC} = 4.5V; V _{EE} = -4.5V; I _X , I _Y , I _Z = 1mA; V _X , V _Y , V _Z = 3.5V		+25°C	50		80	Ω
				C, E, A			100	
Switch On-Resistance Match Between Channels (Note 3)	ΔR _{ON}	V _{CC} = 4.5V; V _{EE} = -4.5V; I _X , I _Y , I _Z = 1mA; V _X , V _Y , V _Z = 3.5V		+25°C	1		4	Ω
				C, E, A			6	
Switch On-Resistance Flatness (Note 4)	R _{FLAT(ON)}	V _{CC} = 5V; V _{EE} = -5V; I _X , I _Y , I _Z = 1mA; V _X , V _Y , V _Z = 3V, 0V, -3V		+25°C	4		10	Ω
				C, E, A			12	
X ₋ , Y ₋ , Z ₋ Off-Leakage (Note 5)	I _{X(OFF)} , I _{Y(OFF)} , I _{Z(OFF)}	V _{CC} = 5.5V; V _{EE} = -5.5V; V _{X-} , V _{Y-} , V _{Z-} = ±4.5V; V _X , V _Y , V _Z = ∓4.5V		+25°C	-1		+1	nA
				C, E, A	-10		+10	
X, Y, Z Off-Leakage (Note 5)	I _{X(OFF)} , I _{Y(OFF)} , I _{Z(OFF)}	V _{CC} = 5.5V; V _{EE} = -5.5V; V _{X-} , V _{Y-} , V _{Z-} = ±4.5V; V _X , V _Y , V _Z = ∓4.5V	MAX4581	+25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582	+25°C	-1		+1	
			MAX4583	C, E, A	-50		+50	
X, Y, Z On-Leakage (Note 5)	I _{X(ON)} , I _{Y(ON)} , I _{Z(ON)}	V _{CC} = 5.5V; V _{EE} = -5.5V; V _X , V _Y , V _Z = ±4.5V	MAX4581	+25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582	+25°C	-1		+1	
			MAX4583	C, E, A	-50		+50	
DIGITAL I/O								
Logic Input Logic Threshold High	V _{AH} , V _{BH} , V _{CH}			C, E, A	1.5		2.4	V
Logic Input Logic Threshold Low	V _{AL} , V _{BL} , V _{CL}			C, E, A	0.8	1.5		V

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MAX4581/MAX4582/MAX4583

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

($V_{CC} = 4.5V$ to $5.5V$, $V_{EE} = -4.5V$ to $-5.5V$, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP (Note 2)	MAX	UNITS
Input-Current High	I_{AH}, I_{BH}, I_{CH}	$V_A, V_B, V_C = 2.4V$	C, E, A	-1		+1	μA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}	$V_A, V_B, V_C = 0.8V$	C, E, A	-1		+1	μA
SWITCH DYNAMIC CHARACTERISTICS							
Inhibit Turn-On Time	t_{ON}	$V_{X_}, V_{Y_}, V_{Z_} = 3V$; $R_L = 300\Omega$; $C_L = 35pF$; Figure 3	$T_A = +25^\circ C$ C, E, A		100 200	200	ns
Inhibit Turn-Off Time	t_{OFF}	$V_{X_}, V_{Y_}, V_{Z_} = 3V$; $R_L = 300\Omega$; $C_L = 35pF$; Figure 3	$T_A = +25^\circ C$ C, E, A		40 150	100	ns
Address Transition Time	t_{TRANS}	$V_{X_}, V_{Y_}, V_{Z_} = \pm 3V$; $R_L = 300\Omega$; $C_L = 35pF$; Figure 2	$T_A = +25^\circ C$ C, E, A		90 200	200	ns
Break-Before-Make Time	t_{BBM}	$V_{X_}, V_{Y_}, V_{Z_} = 3V$; $R_L = 300\Omega$; $C_L = 35pF$; Figure 4	$T_A = +25^\circ C$	4	20		ns
Charge Injection (Note 6)	Q	$C = 1nF$, $R_S = 0\Omega$, $V_S = 0V$	$T_A = +25^\circ C$		0.5	5	pC
Input Off-Capacitance	$C_{X(OFF)}, C_{Y(OFF)}, C_{Z(OFF)}$	$V_{X_}, V_{Y_}, V_{Z_} = 0V$; $f = 1MHz$; Figure 7	$T_A = +25^\circ C$		4		pF
Output Off-Capacitance	$C_{X(OFF)}, C_{Y(OFF)}, C_{Z(OFF)}$	$V_{X_}, V_{Y_}, V_{Z_} = 0V$; $f = 1MHz$; Figure 7	$T_A = +25^\circ C$	MAX4581	18		pF
				MAX4582	10		
				MAX4583	6		
Output On-Capacitance	$C_{X(ON)}, C_{Y(ON)}, C_{Z(ON)}$	$V_{X_}, V_{Y_}, V_{Z_} = 0V$; $f = 1MHz$; Figure 7	$T_A = +25^\circ C$	MAX4581	25		pF
				MAX4582	17		
				MAX4583	12.5		
Off-Isolation	V_{ISO}	$R_L = 50\Omega$, $f = 1MHz$, Figure 6	$T_A = +25^\circ C$		-74		dB
Channel-to-Channel Crosstalk	V_{CT}	$R_L = 50\Omega$, $f = 1MHz$, Figure 6	MAX4581	$T_A = +25^\circ C$	-78		dB
			MAX4582	$T_A = +25^\circ C$	-96		
			MAX4583	$T_A = +25^\circ C$	-73		pF
Total Harmonic Distortion	THD	$R_L = 600\Omega$, $5Vp-p$, $f = 20Hz$ to $20kHz$	$T_A = +25^\circ C$		0.02		%
POWER SUPPLY							
Power-Supply Range	V_{CC}, V_{EE}		C, E, A	± 2		± 6	V
Power-Supply Current	I_{CC}, I_{EE}	$V_{CC} = 5.5V$, $V_{EE} = -5.5V$, $V_A, V_B, V_C, V_{Enable} = V+$ or 0	$T_A = +25^\circ C$	-1		+1	μA
			C, E, A	-10		+10	

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ELECTRICAL CHARACTERISTICS—Single +5V Supply

($V_{CC} = 4.5V$ to $5.5V$, $V_{EE} = 0V$, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN TYP MAX (Note 2)		UNITS
ANALOG SWITCH							
Analog-Signal Range	$V_{X-}, V_{Y-}, V_{Z-}, V_X, V_Y, V_Z$			C, E, A	V_{EE}	V_{CC}	V
Switch On-Resistance	R_{ON}	$V_{CC} = 4.5V$; $I_X, I_Y, I_Z = 1mA$; $V_X, V_Y, V_Z = 3.5V$		$T_A = +25^{\circ}C$ C, E, A	90	150 200	Ω
Switch On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	$V_{CC} = 4.5V$; $I_X, I_Y, I_Z = 1mA$; $V_X, V_Y, V_Z = 3.5V$		$T_A = +25^{\circ}C$ C, E, A	2	8 10	Ω
X_{-}, Y_{-}, Z Off-Leakage (Note 5)	$I_{X(OFF)}, I_{Y(OFF)}, I_{Z(OFF)}$	$V_{CC} = 5.5V$; $V_{X-}, V_{Y-}, V_{Z-} = 1V, 4.5V$; $V_X, V_Y, V_Z = 4.5V, 1V$		$T_A = +25^{\circ}C$ C, E, A	-1 -10	+1 +10	nA
X, Y, Z Off-Leakage (Note 5)	$I_{X(OFF)}, I_{Y(OFF)}, I_{Z(OFF)}$	$V_{CC} = 5.5V$; $V_{X-}, V_{Y-}, V_{Z-} = 1V, 4.5V$; $V_X, V_Y, V_Z = 4.5V, 1V$	MAX4581	$T_A = +25^{\circ}C$ C, E, A	-2 -100	+2 +100	nA
			MAX4582	$T_A = +25^{\circ}C$ C, E, A	-1 -50	+1 +50	
			MAX4583				
X, Y, Z On-Leakage (Note 5)	$I_{X(ON)}, I_{Y(ON)}, I_{Z(ON)}$	$V_{CC} = 5.5V$; $V_X, V_Y, V_Z = 4.5V, 1V$	MAX4581	$T_A = +25^{\circ}C$ C, E, A	-2 -100	+2 +100	nA
			MAX4582	$T_A = +25^{\circ}C$ C, E, A	-1 -50	+1 +50	
			MAX4583				
DIGITAL I/O							
Logic Input Logic Threshold High	$V_{AH}, V_{BH}, V_{CH}, V_{ENABLEH}$			C, E, A	1.5	2.4	V
Logic Input Logic Threshold Low	$V_{AL}, V_{BL}, V_{CL}, V_{ENABLEL}$			C, E, A	0.8	1.5	V
Input-Current High	$I_{AH}, I_{BH}, I_{CH}, I_{ENABLEH}$	$V_{AL}, V_{BL}, V_{CL}, V_{EnableL} = 2.4V$		C, E, A	-1	+1	μA
Input-Current Low	$I_{AL}, I_{BL}, I_{CL}, I_{ENABLEL}$	$V_{AL}, V_{BL}, V_{CL}, V_{EnableL} = 0.8V$		C, E, A	-1	+1	μA
SWITCH DYNAMIC CHARACTERISTICS							
Charge Injection (Note 6)	Q	$C = 1nF, R_S = 0\Omega, V_S = 2.5V$		$T_A = +25^{\circ}C$	0.8	5	pC
Enable Turn-On Time	$t_{(ON)}$	$V_{X-}, V_{Y-}, V_{Z-} = 3V, R_L = 300\Omega, C_L = 35pF$, Figure 3		$T_A = +25^{\circ}C$ C, E, A	100	200 250	ns
Enable Turn-Off Time	$t_{(OFF)}$	$V_{X-}, V_{Y-}, V_{Z-} = 3V, R_L = 300\Omega, C_L = 35pF$, Figure 3		$T_A = +25^{\circ}C$ C, E, A	40	100 150	ns
Address Transition Time	t_{TRANS}	$V_{X-}, V_{Y-}, V_{Z-} = 3V/0V, R_L = 300\Omega, C_L = 35pF$, Figure 2		$T_A = +25^{\circ}C$ C, E, A	80	200 250	ns
Break-Before-Make Time	t_{BBM}	$V_{X-}, V_{Y-}, V_{Z-} = 3V, R_L = 300\Omega, C_L = 35pF$, Figure 4		$T_A = +25^{\circ}C$	10	30	ns
POWER SUPPLY							
Power-Supply Range	V_{CC}, V_{EE}			C, E, A	2	12	V
Power-Supply Current	I_{CC}, I_{EE}	$V_{CC} = 3.6V$; $V_A, V_B, V_C, V_{Enable} = V_+ \text{ or } 0$		$T_A = +25^{\circ}C$	-1	+1	μA
				C, E, A	-10	+10	

Low-Voltage, CMOS Analog Multiplexers/Switches

MAX4581/MAX4582/MAX4583

ELECTRICAL CHARACTERISTICS—Single +3V Supply

($V_{CC} = 2.7V$ to $3.6V$, $V_{EE} = 0V$, $V_{IH} = 2.0V$, $V_{IL} = 0.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog-Signal Range	V _X -, V _Y -, V _Z -, V _X , V _Y , V _Z			C, E, A	V _{EE}		V _{CC}	V
Switch On-Resistance	R _{ON}	V _{CC} = 2.7V; I _X , I _Y , I _Z = 0.1mA; V _X , V _Y , V _Z = 1.5V		T _A = +25°C	190	450	Ω	
				C, E, A		550		
X ₋ , Y ₋ , Z ₋ Off-Leakage (Note 5)	I _X (OFF), I _Y (OFF), I _Z (OFF)	V _{CC} = 3.6V; V _X -, V _Y -, V _Z - = 1V, 3V; V _X , V _Y , V _Z = 3V, 1V		T _A = +25°C	-1	+1	nA	
				C, E, A	-10	+10		
X, Y, Z Off-Leakage (Note 6)	I _X (OFF), I _Y (OFF), I _Z (OFF)	V _{CC} = 3.6V; V _X -, V _Y -, V _Z - = 1V, 3.0V; V _X , V _Y , V _Z = 3.0V, 1V	MAX4581	T _A = +25°C	-2	+2	nA	
				C, E, A	-100	+100		
				MAX4582 MAX4583	T _A = +25°C	-1		+1
					C, E, A	-50		+50
X, Y, Z On-Leakage (Note 6)	I _X (ON), I _Y (ON), I _Z (ON)	V _{CC} = 3.6V; V _X , V _Y , V _Z = 3.0V, 1V	MAX4581	T _A = +25°C	-2	+2	nA	
				C, E, A	-100	+100		
				MAX4582 MAX4583	T _A = +25°C	-1		+1
					C, E, A	-50		+50
DIGITAL I/O								
Logic Input Logic Threshold High	V _{AH} , V _{BH} , V _{CH} , V _{ENABLEH}			C, E, A		1.0	2.0	V
Logic Input Logic Threshold Low	V _{AL} , V _{BL} , V _{CL} , V _{ENABLEL}			C, E, A	0.5	1.0		V
Input-Current High	I _{AH} , I _{BH} , I _{CH} , I _{ENABLEH}	V _A , V _B , V _C = V _{Enable} = 2.0V		C, E, A	-1		+1	μA
Input-Current Low	I _{AL} , I _{BL} , I _{CL} , I _{ENABLEL}	V _A , V _B , V _C = V _{Enable} = 0.5V		C, E, A	-1		+1	μA
SWITCH DYNAMIC CHARACTERISTICS (Note 6)								
Enable Turn-On Time	t _(ON)	V _X -, V _Y -, V _Z - = 1.5V; R _L = 300Ω; C _L = 35pF; Figure 3		T _A = +25°C	170	300	ns	
				C, E, A		400		
Enable Turn-Off Time	t _(OFF)	V _X -, V _Y -, V _Z - = 1.5V; R _L = 300Ω; C _L = 35pF; Figure 3		T _A = +25°C	50	200	ns	
				C, E, A		300		
Address Transition Time	t _{TRANS}	V _X -, V _Y -, V _Z - = 1.5V/0V; R _L = 300Ω; C _L = 35pF; Figure 2		T _A = +25°C	130	300	ns	
				C, E, A		400		
Break-Before-Make Time	t _{BBM}	V _X -, V _Y -, V _Z - = 1.5V; R _L = 300Ω; C _L = 35pF		T _A = +25°C	15	40	ns	
POWER SUPPLY								
Power-Supply Current	I _{CC} , I _{EE}	V _{CC} = 3.6V, V _A , V _B , V _C , V _{Enable} = V ₊ or 0		T _A = +25°C	-1	+1	μA	
				C, E, A	-10	+10		

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., $V_{X_}, V_{Y_}, V_{Z_} = 3V$ to 0 and 0 to -3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at $T_A = +25^\circ C$.

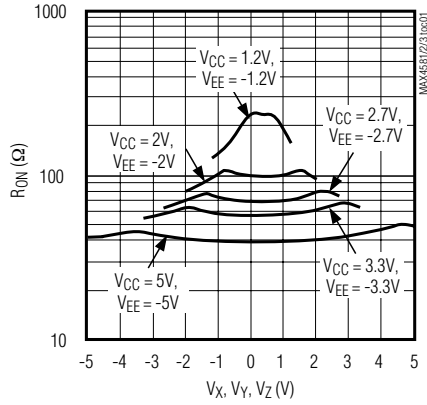
Note 6: Guaranteed by design, not production tested.

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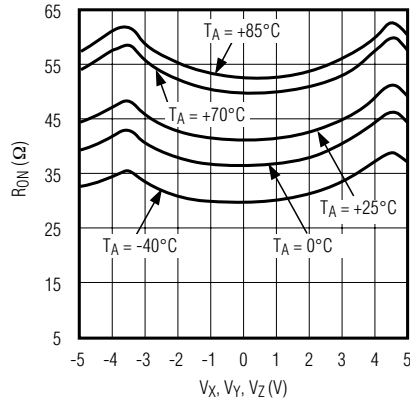
Typical Operating Characteristics

($V_{CC} = 5V$, $V_{EE} = -5V$, $GND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

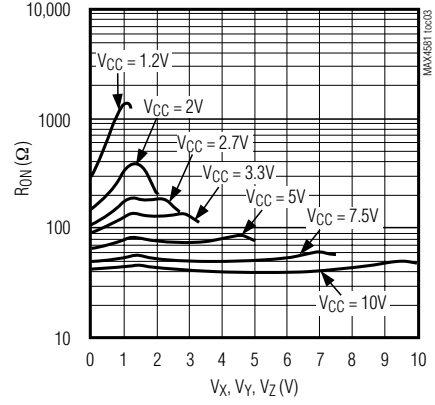
**ON-RESISTANCE vs. V_X , V_Y , V_Z
(DUAL SUPPLIES)**



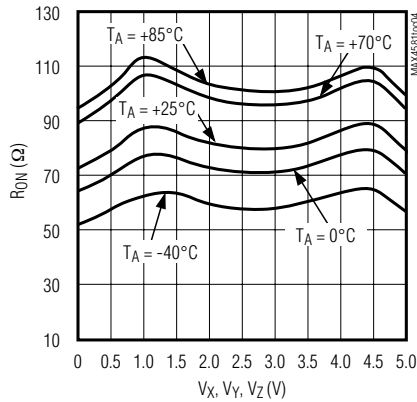
**ON-RESISTANCE
vs. V_X , V_Y , V_Z AND TEMPERATURE
(DUAL SUPPLIES)**



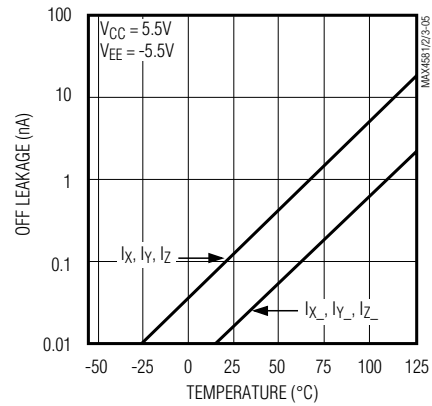
**ON-RESISTANCE vs. V_X , V_Y , V_Z
(SINGLE SUPPLY)**



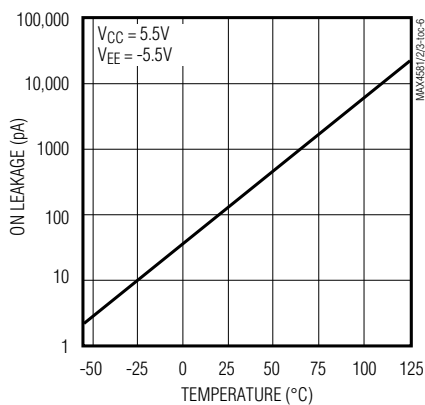
**ON-RESISTANCE
vs. V_X , V_Y , V_Z AND TEMPERATURE
(SINGLE SUPPLY)**



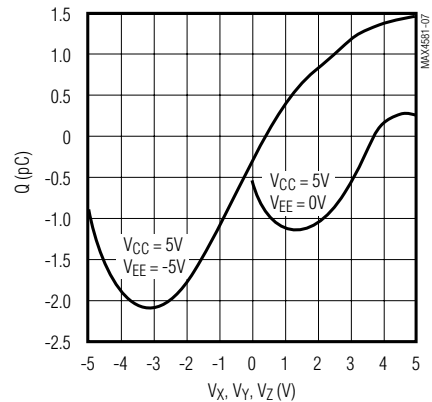
**OFF-LEAKAGE
vs. TEMPERATURE**



**ON-LEAKAGE
vs. TEMPERATURE**



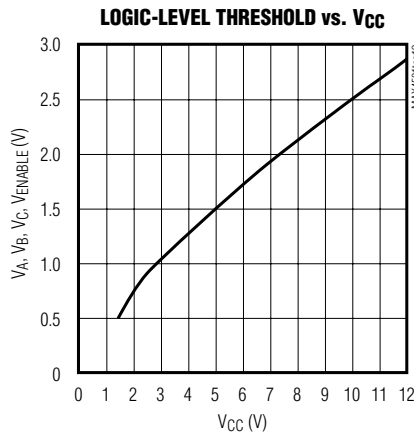
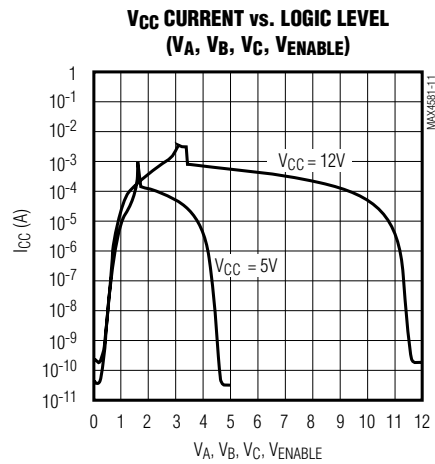
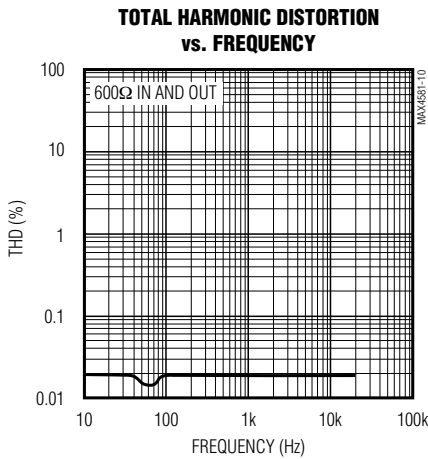
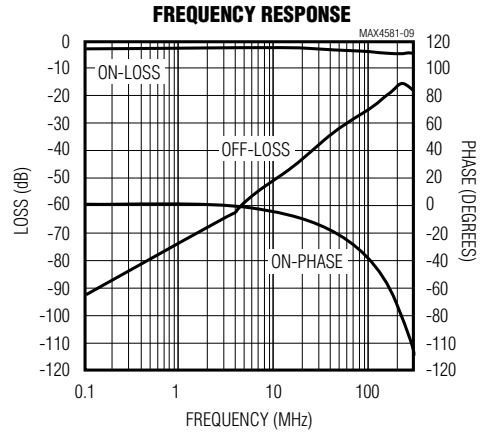
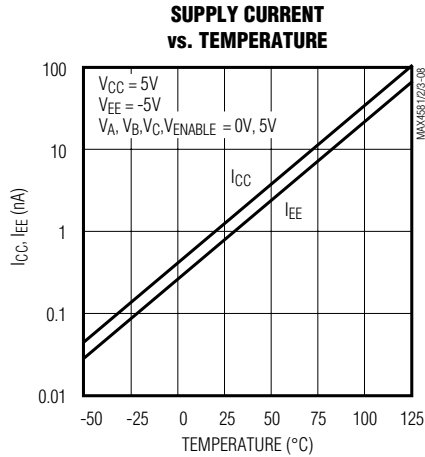
CHARGE INJECTION vs. V_X , V_Y , V_Z



Low-Voltage, CMOS Analog Multiplexers/Switches

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = -5V$, $GND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX4581/MAX4582/MAX4583

Low-Voltage, CMOS Analog Multiplexers/Switches

Pin Description

PIN						NAME	FUNCTION
MAX4581		MAX4582		MAX4583			
DIP, SO, TSSOP	QFN	DIP, SO, TSSOP	QFN	DIP, SO, TSSOP	QFN		
13, 14, 15, 12, 1, 5, 2, 4	11, 12, 13, 10, 15, 3, 16, 2	—	—	—	—	X0–X7	Analog Switch Inputs 0–7
3	1	13	11	14	12	X	Analog Switch “X” Output
—	—	12, 14, 15, 11	10, 12, 13, 9	—	—	X0, X1, X2, X3	Analog Switch “X” Inputs 0–3
—	—	1, 5, 2, 4	15, 3, 16, 2	—	—	Y0, Y1, Y2, Y3	Analog Switch “Y” Inputs 0–3
—	—	3	1	15	13	Y	Analog Switch “Y” Output
—	—	—	—	13	11	X1	Analog Switch “X” Normally Open Input
—	—	—	—	12	10	X0	Analog Switch “X” Normally Closed Input
—	—	—	—	1	15	Y1	Analog Switch “Y” Normally Open Input
—	—	—	—	2	16	Y0	Analog Switch “Y” Normally Open Input
—	—	—	—	3	1	Z1	Analog Switch “Z” Normally Open Input
—	—	—	—	5	3	Z0	Analog Switch “Z” Normally Open Input
—	—	—	—	4	2	Z	Analog Switch “Z” Output
16	14	16	14	16	14	VCC	Positive Analog and Digital Supply-Voltage Input
11	9	10	8	11	9	A	Digital Address “A” Input
10	8	9	7	10	8	B	Digital Address “B” Input
9	7	—	—	9	7	C	Digital Address “C” Input
8	6	8	6	8	6	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to VCC and VEE.)
7	5	7	5	7	5	VEE	Negative Analog Supply-Voltage Input. Connect to GND for single-supply operation.
6	4	6	4	6	4	ENABLE	Digital Enable Input. Normally connected to GND.
—	EP	—	EP	—	EP	EP	Exposed Pad. Connect EP to VCC.

Note: Input and output pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

Applications Information

Power-Supply Considerations

Overview

The MAX4581/MAX4582/MAX4583 construction is typical of most CMOS analog switches. They have three

supply pins: VCC, VEE, and GND. VCC and VEE are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both VCC and VEE. If any analog signal exceeds VCC or VEE, one of these diodes

Low-Voltage, CMOS Analog Multiplexers/Switches

MAX4581/MAX4582/MAX4583

Table 1. Truth Table/Switch Programming

ENABLE INPUT	SELECT INPUTS			ON SWITCHES		
	C*	B	A	MAX4581	MAX4582	MAX4583
H	X	X	X	All switches open	All switches open	All switches open
L	L	L	L	X-X0	X-X0, Y-Y0	X-X0, Y-Y0, Z-Z0
L	L	L	H	X-X1	X-X1, Y-Y1	X-X1, Y-Y0, Z-Z0
L	L	H	L	X-X2	X-X2, Y-Y2	X-X0, Y-Y1, Z-Z0
L	L	H	H	X-X3	X-X3, Y-Y3	X-X1, Y-Y1, Z-Z0
L	H	L	L	X-X4	X-X0, Y-Y0	X-X0, Y-Y0, Z-Z1
L	H	L	H	X-X5	X-X1, Y-Y1	X-X1, Y-Y0, Z-Z1
L	H	H	L	X-X6	X-X2, Y-Y2	X-X0, Y-Y1, Z-Z1
L	H	H	H	X-X7	X-X3, Y-Y3	X-X1, Y-Y1, Z-Z1

X = Don't care

*C not present on MAX4582.

Note: Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from VCC or VEE.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either VCC or VEE and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the VCC and VEE pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can

show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND.

VCC and GND power the internal logic and logic-level translators, and set the input logic limits. The logic-level translators convert the logic levels into switched VCC and VEE signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies and signals and the analog supplies. VCC and VEE have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when VCC is +5V. As VCC rises, the threshold increases

Low-Voltage, CMOS Analog Multiplexers/Switches

slightly, so when V_{CC} reaches +12V the threshold is about 3.1V (above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs).

Bipolar Supplies

These devices operate with bipolar supplies between $\pm 2V$ and $\pm 5V$. The V_{CC} and V_{EE} supplies need not be symmetrical, but their sum cannot exceed the +13V absolute maximum rating.

Single Supply

These devices operate from a single supply between +2V and +12V when V_{EE} is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually “work” with a single supply near or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, then V_{EE} , followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog-signal range to one diode drop below V_{CC} and one diode drop above V_{EE} , but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V_{CC} and V_{EE} should not exceed 13V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -50dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also degrade off isolation. Adjacent channel attenuation is about 3dB above that of a bare IC socket and is entirely due to capacitive coupling.

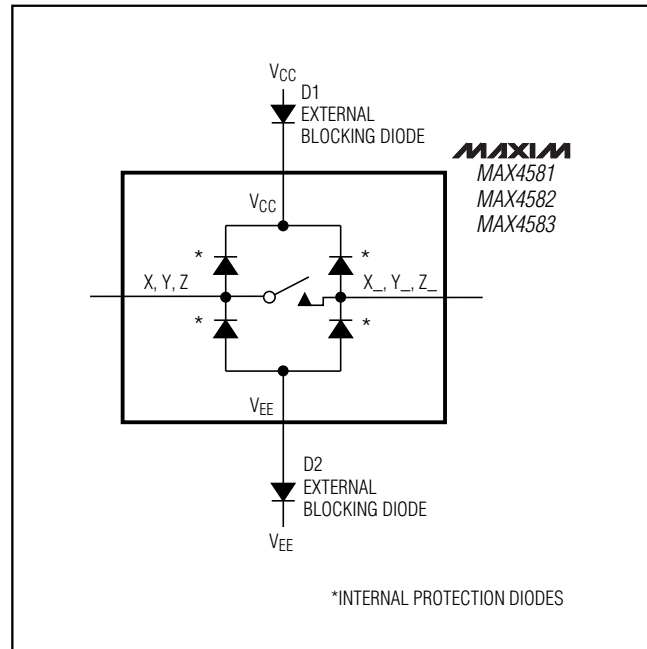


Figure 1. Overvoltage Protection Using External Blocking Diodes

Pin Nomenclature

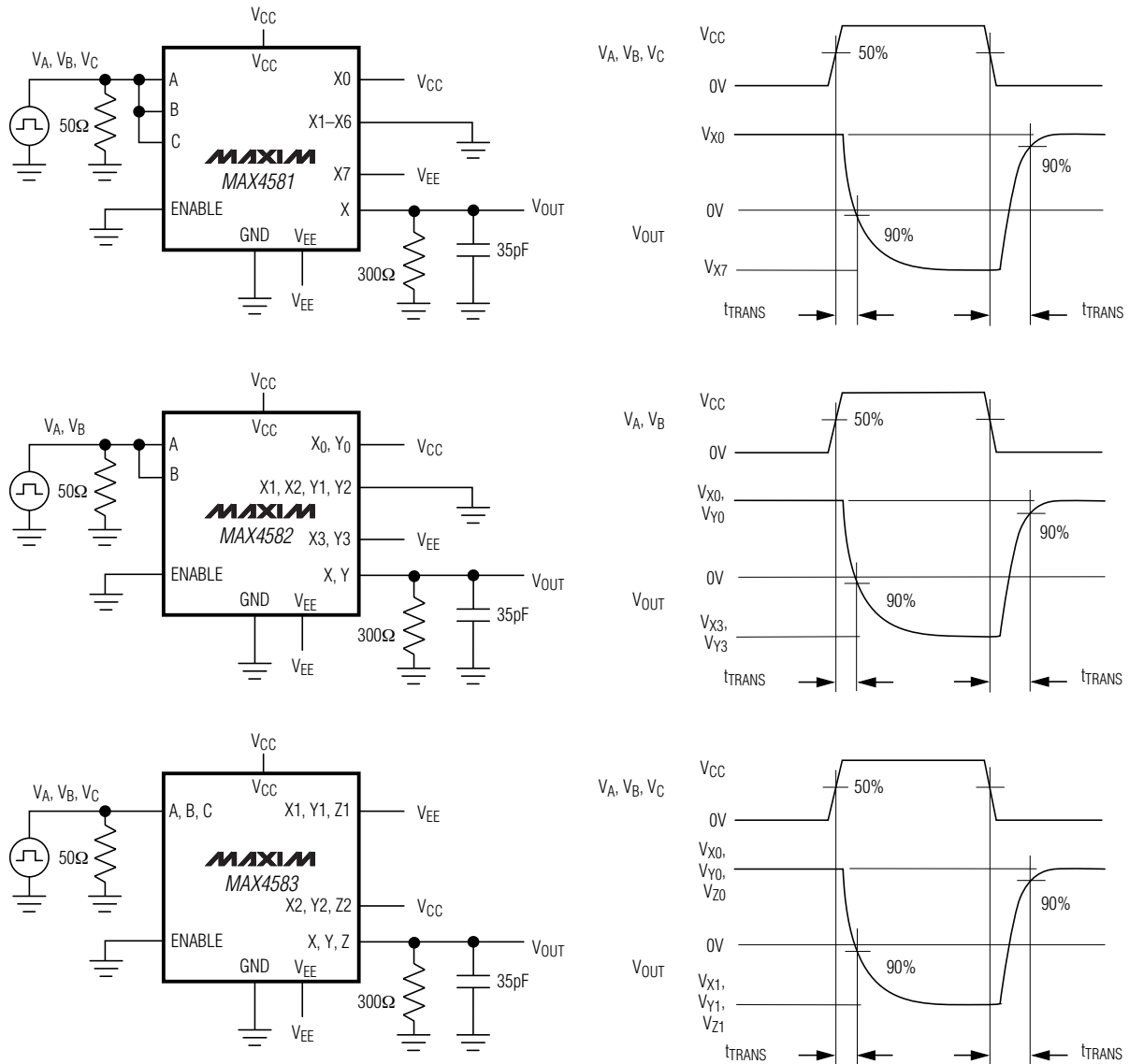
The MAX4581/MAX4582/MAX4583 are pin-compatible with the industry-standard 74HC4051/74HC4052/74HC4053 and the MAX4051/MAX4052/MAX4053. They function identically and have identical logic diagrams, although these parts differ electrically.

The pin designations and logic diagrams in this data sheet conform to the original 1972 specifications published by RCA for the CD4051/CD4052/CD4053. These designations differ from the standard Maxim switch and mux designations as found all other Maxim data sheets (including the MAX4051/MAX4052/MAX4053) and may cause confusion. Designers who feel more comfortable with Maxim's standard designations are advised that the pin designations and logic diagrams on the MAX4051/MAX4052/MAX4053 data sheet may be freely applied to the MAX4581/MAX4582/MAX4583.

Low-Voltage, CMOS Analog Multiplexers/Switches

Test Circuits/Timing Diagrams

MAX4581/MAX4582/MAX4583



$V_{EE} = 0\text{V}$ FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

Figure 2. Address Transition Times

The diagram shows a MAX4581 monostable multivibrator. The input section has three pins labeled A, B, and C, which are connected to a common input node. This node is driven by a square wave pulse source labeled V_{ENABLE} through a 50Ω resistor. The output section has a pin labeled X, which is connected to an output node. This node is loaded with a 300Ω resistor and a 35pF capacitor in parallel. The output voltage is labeled V_{OUT} . The device is powered by V_{CC} and V_{EE} pins, both of which are connected to ground. The chip is labeled "MAXIM MAX4581".

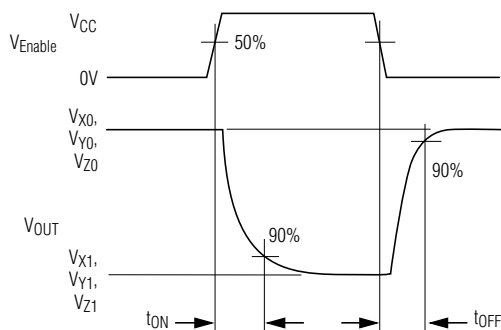
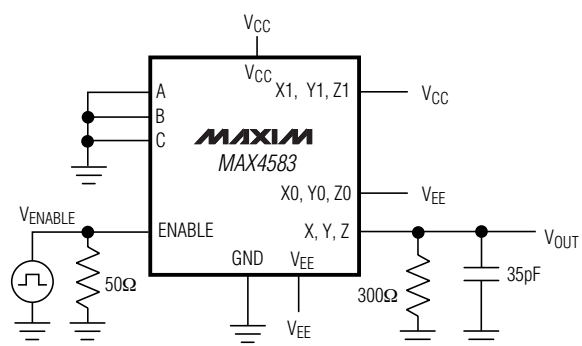
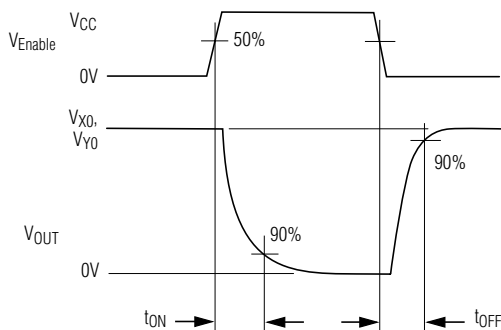
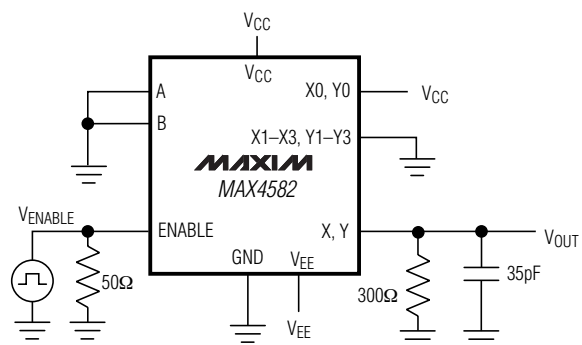
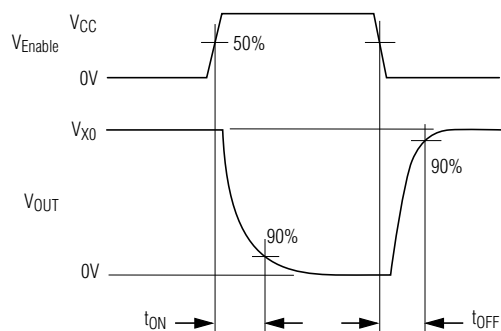


Figure 3. Inhibit Switching Times

Low-Voltage, CMOS Analog Multiplexers/Switches

Test Circuits/Timing Diagrams (continued)

MAX4581/MAX4582/MAX4583

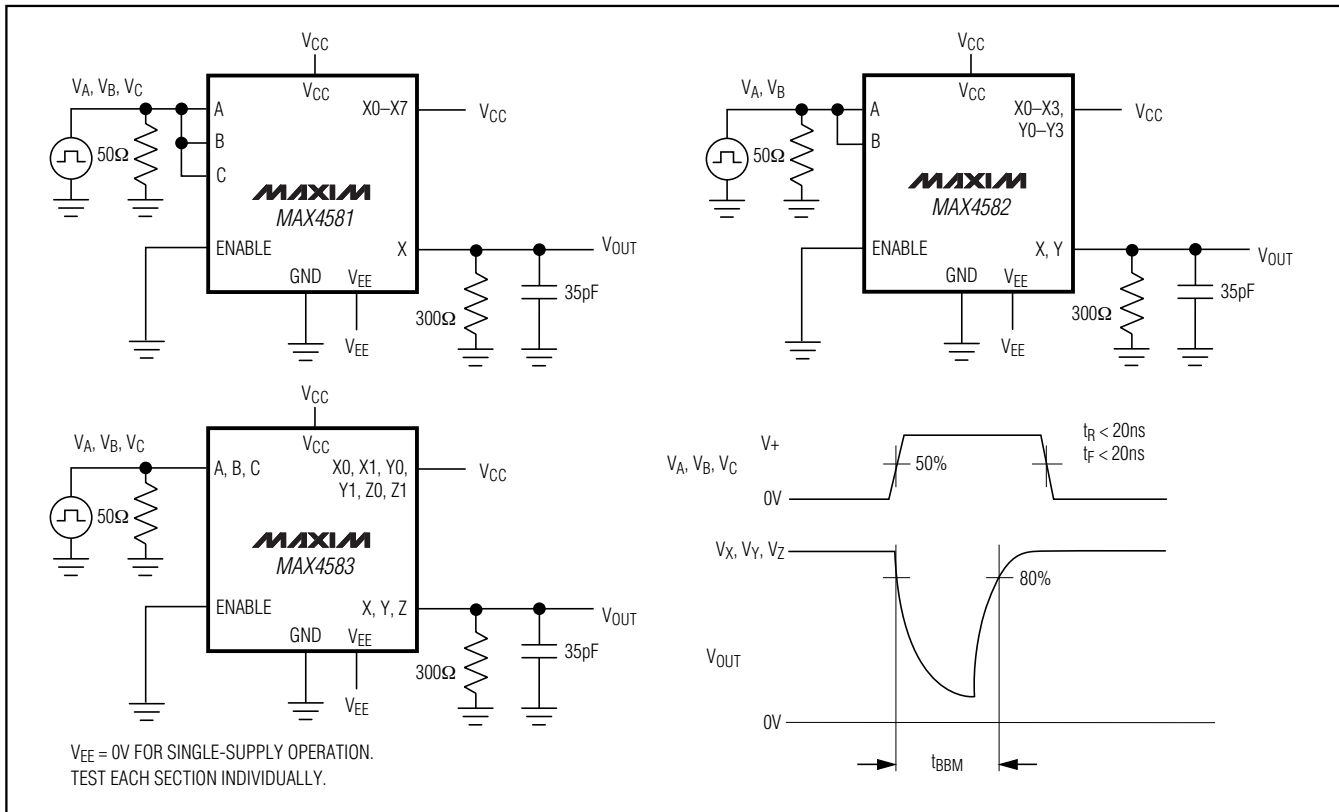


Figure 4. Break-Before-Make Interval

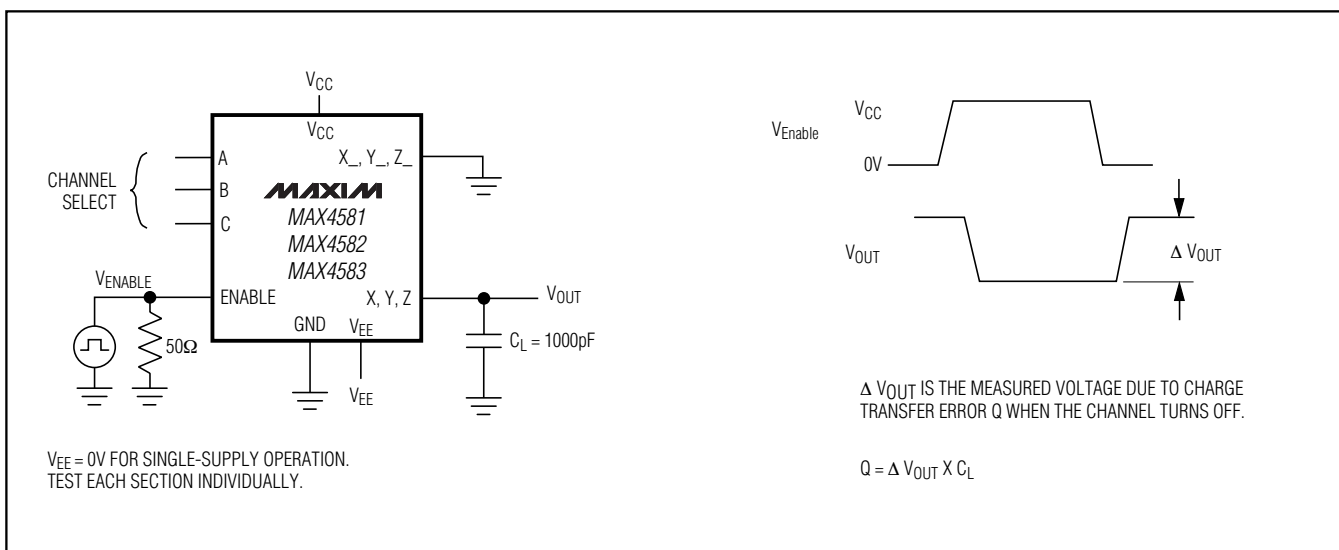


Figure 5. Charge Injection

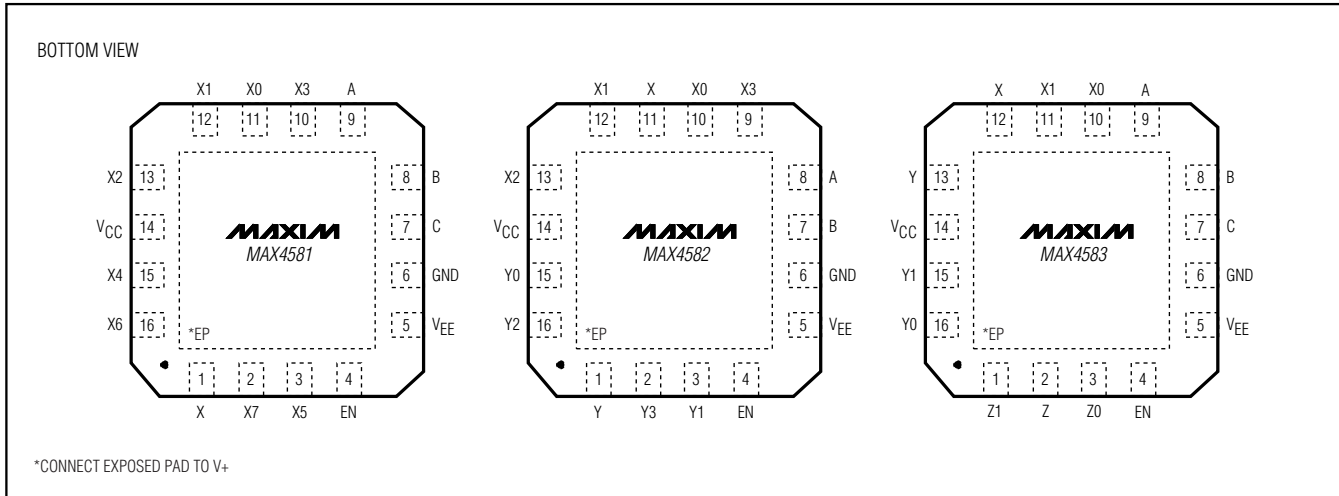
MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
 OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
 ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
 CROSSTALK (MAX4582/MAX4583) IS MEASURED FROM ONE CHANNEL (A, B, C) TO ALL OTHER CHANNELS.
 SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

The diagram illustrates the MAX4581, MAX4582, and MAX4583 capacitive touch controller. The chip is shown with its pins: VCC, GND, VEE, and ENABLE. The CHANNEL SELECT pins (A, B, C) are connected to a common ground. The X, Y, Z pins are connected to a 1MHz CAPACITANCE ANALYZER. The chip is labeled MAX4581, MAX4582, and MAX4583.

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Low-Voltage, CMOS Analog Multiplexers/Switches

Pin Configurations/Functional Diagrams (continued)



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4581CEE	0°C to +70°C	16 QSOP	E16-4
MAX4581C/D	0°C to +70°C	Dice*	—
MAX4581EPE	-40°C to +85°C	16 Plastic DIP	P16-1
MAX4581ESE	-40°C to +85°C	16 Narrow SO	S16-2
MAX4581EUE	-40°C to +85°C	16 TSSOP	U16-2
MAX4581EEE	-40°C to +85°C	16 QSOP	E16-4
MAX4581EGE	-40°C to +85°C	16 QFN – EP**	G1644-1
MAX4581ASE	0°C to +70°C	16 Narrow SO	S16-2
MAX4581AUE	0°C to +70°C	16 TSSOP	U16-2
MAX4582CPE	0°C to +70°C	16 Plastic DIP	P16-1
MAX4582CSE	0°C to +70°C	16 Narrow SO	S16-2
MAX4582CUE	0°C to +70°C	16 TSSOP	U16-2
MAX4582CEE	-40°C to +85°	16 QSOP	E16-4
MAX4582C/D	-40°C to +85°	Dice*	—
MAX4582EPE	-40°C to +85°	16 Plastic DIP	P16-1
MAX4582ESE	-40°C to +85°	16 Narrow SO	S16-2
MAX4582EUE	-40°C to +85°	16 TSSOP	U16-2

*Contact factory for availability.

**EP = Exposed pad.

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4582EEE	-40°C to +85°	16 QSOP	E16-4
MAX4582EGE	-40°C to +85°	16 QFN – EP**	G1644-1
MAX4582ASE	0°C to +70°C	16 Narrow SO	S16-2
MAX4582AUE	0°C to +70°C	16 TSSOP	U16-2
MAX4583CPE	0°C to +70°C	16 Plastic DIP	P16-1
MAX4583CSE	0°C to +70°C	16 Narrow SO	S16-2
MAX4583CUE	0°C to +70°C	16 TSSOP	U16-2
MAX4583CEE	0°C to +70°C	16 QSOP	E16-4
MAX4583C/D	0°C to +70°C	Dice*	—
MAX4583EPE	-40°C to +85°	16 Plastic DIP	P16-1
MAX4583ESE	-40°C to +85°	16 Narrow SO	S16-2
MAX4583EUE	-40°C to +85°	16 TSSOP	U16-2
MAX4583EEE	-40°C to +85°	16 QSOP	E16-4
MAX4583EGE	-40°C to +85°	16 QFN – EP**	G1644-1
MAX4583ASE	-40°C to +125°	16 Narrow SO	S16-2
MAX4583AUE	-40°C to +125°	16 TSSOP	U16-2

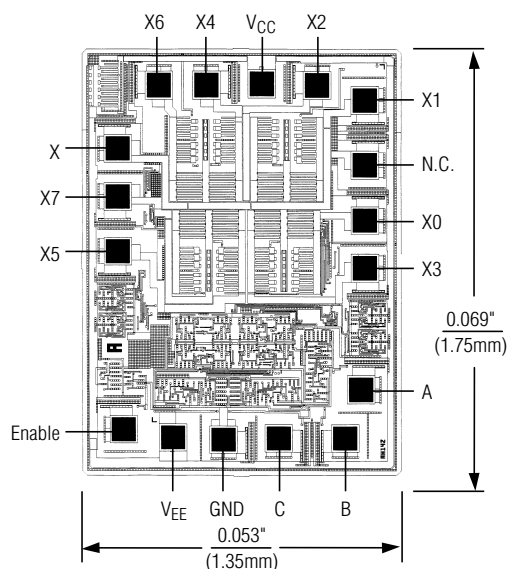
MAX4581/MAX4582/MAX4583

Chip Topographies (continued)

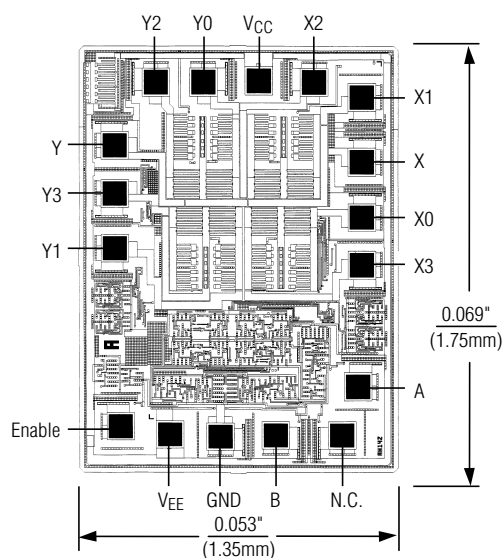
Low-Voltage, CMOS Analog Multiplexers/Switches

Chip Topographies

MAX4581



MAX4582

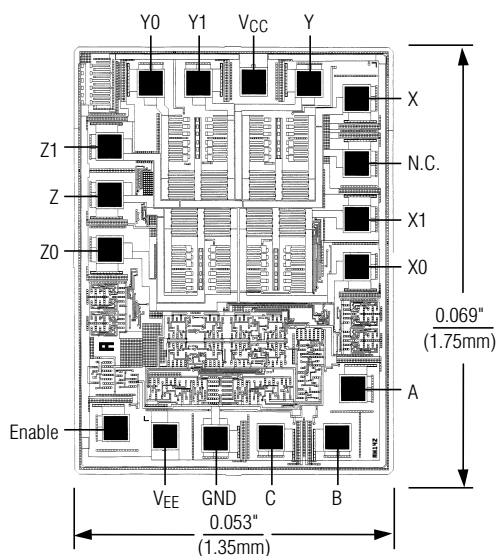


N.C. = NO CONNECTION

TRANSISTOR COUNT: 219
SUBSTRATE CONNECTED TO V₊.

TRANSISTOR COUNT: 219
SUBSTRATE CONNECTED TO V₊.

MAX4583



N.C. = NO CONNECTION

TRANSISTOR COUNT: 219
SUBSTRATE CONNECTED TO V₊.

MAX4581/MAX4582/MAX4583

32L QFN.EPS

The drawing illustrates the mechanical specifications of a 16-pin Quad Flat Pack (QFN) package. It includes three main views: a top view, a bottom view, and a cross-sectional view labeled 'SECTION "C-C"'. The top view shows the package footprint with dimensions for overall width (A), pin pitch (D), and pin width (E). It also indicates the location of the tie bar (N) and the terminal tips. The bottom view shows the underside of the package, highlighting the seating plane (C) and the dimensions for the tie bar (N) and the terminal tips. The cross-sectional view shows the internal structure of the package, including the die (D), the die attach (A), and the solder (S). Dimensions for the die thickness (D), the die attach thickness (A), and the solder thickness (S) are provided. The drawing also includes callouts for the terminal tips and the tie bar, indicating that the dimensions are for the odd terminal/side and the even terminal/side.

TOP VIEW

BOTTOM VIEW

SECTION "C-C"
SCALE: NONE

FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE

STANDARD DETAIL A
PIN #1 ID AND TIE BAR MARK OPTIONS

PROPRIETARY INFORMATION	
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM	
APPROVAL	DOCUMENT CONTROL NO. 21-0091
REV. 1	1/2

Low-Voltage, CMOS Analog Multiplexers/Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
ø	0"		12"	0"		12"	0"		12"	0"		12"

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. — 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0091	1	2/2

Revision History

Pages changed at Rev 5: 1, 8, 15, 16, 18

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